**In the Claims:**

1. (Currently Amended) A field-effect transistor ~~(222)~~,

having a doped channel region arranged along a depression ~~(72)~~,

having a doped terminal region ~~(16)~~ near an opening of the depression ~~(72)~~,

having a doped terminal region ~~(18)~~ remote from the opening,

having a control region ~~(172)~~ arranged in the depression ~~(72)~~,

and having an electrical insulating region ~~(170)~~ between the control region ~~(172)~~ and the channel region,

the terminal region ~~(18, 54)~~ remote from the opening leading as far as a surface containing the opening or being electrically conductively connected to an electrically conductive connection leading to the surface, the field-effect transistor being a drive transistor at a word line or at a bit line of a memory cell array, the field-effect transistor comprising only one depression in which the control region is arranged.

2. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 1, wherein the terminal regions ~~(16, 18)~~ contain the same dopant concentration and dopants of the same conduction type.

3. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 1 ~~or 2~~, wherein the channel region has a length ~~(l)~~ corresponding to at least two thirds of ~~the~~ a depth of the depression ~~(72)~~.

4. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 1 ~~one of the preceding claims~~, wherein the depression is a trench ~~(72)~~ or a hole.

5. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 4 ~~one of the preceding claims~~, wherein the channel region lies on ~~both~~ opposing sides of the trench ~~(72)~~ or along ~~the~~ an entire periphery of the hole.

6. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 4 ~~one of claims 1 to 4~~, wherein the channel region lies only on one side of the trench ~~(72)~~ or only along part of ~~the~~ a periphery of the hole.

7. (Cancelled)

8. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 1 ~~one of the preceding claims~~, wherein the depression ~~(72)~~ for the control region and a depression ~~(70, 76)~~ filled with an electrical insulating material between the field-effect transistor ~~(222)~~ and an adjacent electrical component have the same depth.

9. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 1 ~~one of claims 1 to 7~~, wherein the depression ~~(72)~~ for the control region has a smaller depth than a depression ~~(70a, 76a)~~ filled with an electrical insulating material between the field-effect transistor ~~(222)~~ and an adjacent electronic component.

10. (Currently Amended) The field-effect transistor ~~(222)~~ as claimed in claim 1 ~~one of the preceding claims~~, wherein the insulating region ~~(170)~~ has an insulating thickness of at least 15 nm~~, preferably 20 nm,~~

~~and/or wherein the distance (l) between the terminal regions (16, 18) along the depression (72) is at least 0.4 µm,~~

~~and/or wherein at least one terminal region (16, 18) has a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than 9 volts or greater than 15 volts, but preferably less than 30 volts~~.

11-12. (Cancelled)

13. (Currently Amended) A method comprising:

~~for~~ fabricating a field-effect transistor ~~(222), in particular a field-effect transistor (222) as claimed in one of claims 1 to 12,~~ having the following steps to be performed without restriction by the order specified:

provision of a carrier material ~~(10)~~ having a surface to be processed,

formation of a terminal region ~~(16)~~ near the surface and a terminal region ~~(18)~~ remote from the surface,

formation of at least one depression ~~(72)~~, which leads from the terminal region ~~(16)~~ near the surface as far as the terminal region ~~(18)~~ remote from the surface or which leads from a region for the terminal region near the surface to a region for the terminal region remote from the surface, the field-effect transistor comprising only one depression in which a control region is arranged,

production of an electrical insulating layer ~~(170)~~ in the depression ~~(72)~~,

introduction of an electrically conductive control region ~~(172)~~ into the depression ~~(72)~~; and

using the field-effect transistor at a word line or a bit line of a memory cell array.

14. (Currently Amended) The method as claimed in claim 13, wherein the formation of the terminal regions is performed at least one of: before the formation of the depression and/~~or~~ before ~~the~~ filling of the depression ~~(72)~~.

15. (Currently Amended) The method as claimed in claim 13 ~~or 14~~, comprising the following step: formation of a connecting region ~~(54)~~ from the terminal region ~~(18)~~ remote from the surface to ~~the~~ a surface of ~~the~~ a semiconductor layer ~~(10)~~.

16. (Currently Amended) The method as claimed in ~~one of~~ claims 13 ~~to 15~~, wherein at least one insulating depression ~~(70, 74, 76)~~ is formed at the same time as the depression ~~(72)~~ for the control region.

17. (Currently Amended) The method as claimed in claim 16, wherein the insulating depression ~~(70, 74, 76)~~ is formed with the same depth as the depression ~~(72)~~ for the control region.

18. (Currently Amended) The method as claimed in claim 16, wherein the insulating depression ~~(70a, 76a)~~ is made deeper than the depression ~~(72a)~~ for the control region.

19. (Currently Amended) The method as claimed in claim 18, wherein the insulating depression is wider than the depression ~~(72)~~ for the control region at least in an upper section, and wherein the two depressions are formed in a common etching process in which wider depressions are etched ~~considerably~~ more deeply than narrower depressions.

20. (New) The field-effect transistor as claimed in claim 1, wherein at least one of:

a distance between the terminal regions along the depression is at least 0.4 µm, and

at least one terminal region has a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than 9 volts but less than 30 volts.

21. (New) A method of using of a field-effect transistor having a doped channel region arranged along a depression, a doped terminal region near an opening of the depression, a doped terminal region remote from the opening, a control region arranged in the depression, and an electrical insulating region between the control region and the channel region, the terminal region remote from the opening leading as far as a surface containing the opening or being electrically conductively connected to an electrically conductive connection leading to the surface, and comprising only one depression in which the control region is arranged, the method comprising: using the field-effect transistor as a driving transistor at a word line or a bit line of a flash memory of an EEPROM memory module.

22. (New) A method of using of a field-effect transistor having a doped channel region arranged along a depression, a doped terminal region near an opening of the depression, a doped terminal region remote from the opening, a control region arranged in the depression, and an electrical insulating region between the control region and the channel region, the terminal region remote from the opening leading as far as a surface containing the opening or being electrically conductively connected to an electrically conductive connection leading to the surface, and comprising only one depression in which the control region is arranged, the method

comprising: using the field-effect transistor for switching a voltage having a magnitude of greater than 9 volts but less than 30 volts.